SOLE INVENTOR P16220

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Richard Zimmermann

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Tieyu Zheng**, a citizen of China, residing at 3800 West Chandler, Apt. 1083, Chandler, Arizona 85226 have invented a new and useful **LOW-PROFILE PACKAGE FOR HOUSING AN OPTOELECTRONIC ASSEMBLY**, of which the following is a specification.

LOW-PROFILE PACKAGE FOR HOUSING AN OPTOELECTRONIC ASSEMBLY

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation-in-part (CIP) of Application No. 10/444,342, entitled "Package for Housing an Optoelectronic Assembly" filed May 23, 2003.

FIELD OF THE DISCLOSURE

[0002] An optoelectronic assembly and, more specifically, a low-profile package for housing an optoelectronic assembly are disclosed.

BACKGROUND

[0003] Optoelectronic components or active optical devices such as diode lasers, light-emitting diodes (LEDs), and photodiode detectors are used for printing, data storage, optical data transmission and reception, laser pumps, and a multitude of other applications. Most optoelectronic components are typically sealed inside a hermetically sealed package for performance requirements and operational stability. Optoelectronic packages are intended to provide a hermetic structure to protect passive and active optical elements and devices as well as related electrical components from damage resulting from moisture, dirt, heat, radiation, and/or other sources.

[0004] For high-speed applications (e.g., 2 Gbps and above), proper operation of the optical and/or electrical components inside the package may be affected unless careful attention is paid to the packaging of these components. Standard optical module packaging such as that used in optical telecommunication applications requires a hermetic enclosure. Sealed packages are necessary to contain, protect, and electrically connect optoelectronic components. These requirements have resulted in packages that are large, costly, and more difficult to manufacture than typical

electronic packages. In fact, the cost and size of most optoelectronic devices are mainly dominated by the package rather than the optical devices themselves.

[0005] Current designs of optoelectronic packages and associated fabrication processes are not easily adapted for automated manufacturing techniques because conventional packages for optoelectronic components such as large so-called "butterfly" packages are characterized by numerous mechanical parts (submounts, brackets, ferrules, etc.), and three-dimensional (3D) alignment requirements. Butterfly packages are basically can-and-cover type arrangements that contain an optical subassembly mounted to a metallic baseplate, with leads coming out of the sides for electrical connections. The optical subassembly may be built up separately, outside of the can, and then later installed in the can. The circuits within the optical subassembly are wire-bonded to the leads of the butterfly can, which is then sealed with a lid to create a hermetic enclosure. Unfortunately, conventional butterfly cans have a high profile, and are costly and time-consuming to manufacture. In addition, the electrical components require a separate electrical subassembly that is located outside of the butterfly can. The requirement of a separate electrical subassembly that is separate and apart from the optical subassembly inside the butterfly can increases manufacturing costs significantly.

[0006] Transistor-Outline (TO) packages are also commonly used to house optoelectronic components. Conventional TO packages include a generally tall, cylindrical, u-shaped metal cap, and a metal header or base to which the metal cap is attached. In such packages, metal-based bonding techniques such as, for example, fusion welding, are often required to provide a hermetic seal between the metal cap and the header. To weld the metal cap onto the header, the header is typically formed of a metallic material such as Kovar™ or stainless steel. However, it is advantageous to use ceramic bases in connection with high-speed applications because ceramic bases are ideal for RF applications. Particularly, ceramic headers provide easy routing of high-speed circuits. Unfortunately, ceramic is not compatible with metal

with regard to weldability, and therefore has not been widely used as the material for the header or base in conventional TO packages. In addition, because of the u-shaped configuration of the metal caps associated with conventional TO packages, expensive tooling such as, for example, two-piece tooling equipment, is required to manufacture the u-shaped metal caps.

[0007] Typically, when active optical devices (e.g., diode lasers) and integrated circuits adapted to control the active optical devices (e.g., diode drivers) are spaced too far apart from each other, parasitic capacitance, resistance, and/or inductance may affect electrical signals traveling between the components, thus resulting in slower signal propagation speeds. The electrical performance is of particular concern for high-speed applications. Consequently, electrical performance may be improved during high-speed applications when the distance between the active optical device and its associated driving or receiving integrated circuit chip is as short as possible. Although this arrangement may increase signal propagation speed, it may, unfortunately, also increase heat dissipation requirements of the assembly significantly.

[0008] As the power density increases in optoelectronic devices and/or electrical components used in high-speed applications, an optimal heat sink is necessary to dissipate heat efficiently from the optoelectronic device and/or electrical components. Heat sinks are devices capable of dissipating heat away from the optoelectronic and/or electrical components into the surrounding atmosphere by convection. Typical heat sinks may include cooling fins attached to a heat sink base that is in contact with the header or base of the optoelectronic package. The fins of the heat sink may have any shape and size necessary to dissipate heat away from the optoelectronic device and/or electrical components, and may be oriented either parallel or perpendicular relative to the base of the optoelectronic package.

[0009] Commercially available heat sinks are generally square or rectangular in shape. As such, the circular headers of conventional optoelectronic packages require

either modifications to the structural design of the heat sinks to be able to accommodate the circular headers, or manufacturing adjustments to attach the circular header to the square or rectangular heat sink. This configuration results in a complex, slow, and expensive manufacturing process. Additionally, the quality of the contact between the optoelectronic package and the attached heat sink has a great impact on the overall thermal performance. Lower thermal impedance between the optoelectronic package and the heat sink results in higher conductive heat transfer. Therefore, it is advantageous that the header of the optoelectronic package be in intimate, conformal contact with the attached heat sink to optimize the thermal characteristics, which results in increased efficiency.

[0010] In addition, existing optoelectronic packaging techniques often involve manual or semi-automated manufacturing processes. Therefore, to reduce manufacturing costs, it is advantageous to employ automated batch packaging processes that can fabricate a large number of optoelectronic packages simultaneously.

[0011] Currently, there is a great demand for smaller optoelectronic packages to allow for higher density of data transmission. Smaller optoelectronic packages allow the devices (e.g., transceivers) into which the optoelectronic packages are placed to become smaller. Moreover, optoelectronic packages having a lower profile are advantageous due to space limitations of the devices into which the optoelectronic packages are placed. Therefore, a need exists for an optoelectronic package that provides for a more efficient use of limited space, allows for automated fabrication, and that is simple and inexpensive to fabricate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a perspective view of a low-profile package for housing an optoelectronic assembly;

[0013] Fig. 2 is an exploded view of an insulating base, an adhesive layer, and a metal sealing member in accordance with a first embodiment;

[0014] Fig. 3 is an exploded view of the insulating base, the adhesive layer, and the metal sealing member in accordance with a second embodiment; and

[0015] Fig. 4 is an exploded view illustrating the internal components housed inside the low-profile package.

DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

[0016] Referring to Fig. 1, a low-profile package 100 for housing an optoelectronic assembly is shown. The low-profile package 100 includes an insulating base or substrate 110, a metal sealing member 140, and a substantially flat metal cover 150. Preferably, the insulating base 110 is formed of a material with high thermal conductivity for directing dissipated heat away from the optoelectronic assembly. By using a high thermal conductivity material, the insulating base 110 is capable of effectively dissipating the heat of uncooled active optical devices, e.g., diode lasers, and can incorporate integrated circuits, e.g., diode driver chips, into the low-profile optoelectronic package 100.

[0017] In the past, integrated circuit chips have not been integrated into the optoelectronic package 100 because the thermal conductivity of the metallic header of conventional optoelectronic packages was unsuitable for mounting such chips. As discussed in greater detail below, the integrated, low-profile optoelectronic package 100 of the present disclosure, which includes the active optical device 200 and its associated integrated circuit 220 (see Fig. 4) provides a high-speed module that saves power, space, and costs, without sacrificing reliability and performance.

[0018] Suitable materials for the insulating base 110 include ceramics such as alumina, beryllium oxide (BeO), and aluminum nitride (AlN). The insulating base 110 includes an upper surface 120, a lower surface 130, and four substantially flat sidewalls 125 (only two of which are shown) extending downwardly from the upper

surface 120. The thickness of the insulating base 110 may be approximately 1 mm. Of course, it should be understood that the insulating base 110 could be thicker or thinner as desired.

[0019] As shown, both the upper and lower surfaces 120, 130 of the insulating base 110 are substantially planar. It is well known that mounting techniques using planar substrates such as, for example, pick-and-place techniques, are suited to high-volume manufacturing. In addition, because overall mechanical stability is directly related to the stability of the base 110, the substantially planar upper surface 120 of the low-profile optoelectronic package 100 provides good mechanical stability. Furthermore, by using a base 110 made of a material with a coefficient of thermal expansion (CTE) that matches the CTE of the metal sealing member 140 (e.g., a base 110 made of a ceramic with a low CTE), optimal mechanical stability may be obtained.

[0020] Due to the polygonal shape (e.g., square or rectangular) of the insulating base 110, the contact at the mating, heat-conducting surface of the insulating base 110 and a commercially available square or rectangular-shaped heat dissipating device (not shown) may be improved. Preferably, the heat dissipating device is a heat sink. However, other types of heat dissipating devices such as, for example, heat pipes are equally applicable. In this manner, the polygonal shape of the insulating base 110 provides sufficient thermal contact and coupling with a polygonal-shaped (e.g., square or rectangular) heat sink, thereby improving the heat transfer characteristics therebetween. In addition, the substantially flat sidewalls 125 provide a heat dissipation area because the heat generated by the optoelectronic and/or electrical components housed within the low-profile package 100 may be conducted to the substantially flat sidewalls 125. As a result, heat dissipation efficiency is increased. Furthermore, the high thermal conductivity of the ceramic material of the insulating base 110 makes it possible to efficiently extract the heat produced by the optoelectronic device and/or electrical components.

[0021] With reference to Fig. 2, a first plurality of holes or signal vias 117 may be formed through the insulating base 110 by, for example, a mechanical drilling process or a laser machining process. The first plurality of holes 117 is adapted to electrically connect signals from the upper surface 120 of the insulating base 110 to the lower surface 130 of the insulating base 110.

[0022] In a second embodiment illustrated in Fig. 3, a second plurality of holes or vias 115 may be formed through the insulating base 110. The second plurality of holes 115 is adapted to conduct welding current from the substantially flat metal cover 150 to the insulating base 110 when the substantially flat metal cover 150 is hermetically sealed to the insulating base 110 by, for example, a resistance welding technique.

[0023] The insulating base 110 also includes a conductive material layer (not shown) deposited on both the upper and lower surfaces 120, 130 of the insulating base 110. The material layers may be deposited using physical vapor deposition (PVD) techniques such as evaporation, sputtering, screen printing, or other suitable processes. The conductive material may include a metal such as, for example, copper, gold, tin, a copper/tin alloy, tungsten, lead, nickel, palladium, or any other similar metal. Preferably, the metal layers on each of the upper and lower surfaces 120, 130 of the insulating base 110 include a thick film metallization that is capable of being soldered or brazed. In other words, the metal layers include films with a thickness of greater than approximately 10 μm. If desired, however, the metal layers may include a thin film metallization. In any event, the thickness of the metal layers is based, in part, on the requirements for brazing or soldering of the metal sealing member 140 to the upper surface 120 of the insulating base 110.

[0024] The first plurality of holes 117 is, likewise, substantially filled with the same or similar electrically conductive material as that deposited on the upper and lower surfaces 120, 130 of the insulating base 110. For example, the first plurality of

holes 117 may be filled with flowable solder, or screen-filled using a paste of conductive material such as, for example, copper and/or tungsten.

[0025] Similarly, in the second embodiment illustrated in Fig. 3, the first plurality of holes 117 and the second plurality of holes 115 are substantially filled with the same or similar electrically conductive material as that deposited on the upper and lower surfaces 120, 130 of the insulating base 110. In the embodiment of Fig. 3, a metal contact member (not shown) may be attached to the lower metallized surface 130 of the insulating base 110 via an adhesive layer (e.g., a brazing paste or a solder preform layer) disposed between the metal contact member and the lower surface 130 of the insulating base 110. In this manner, the metal contact member is in contact with each of the second plurality of filled holes 115 at the lower surface 130 of the insulating base 110. The metal contact member may be sufficiently etched, grinded, and/or polished to provide a substantially flat contact surface at the lower surface 130 of the insulating base 110.

[0026] The insulating base 110 may be configured as a multilayer substrate having a plurality of levels. Multiple metal layers may be provided at each of the plurality of levels, and joined together (e.g., laminated) on the insulating base 110. In this configuration, the first plurality of holes 117 may be formed in the layers so that signals can be communicated between the adjacent layers.

[0027] The metal layers deposited on the upper and lower surfaces 120, 130 of the insulating base 110 may be patterned to include a plurality of electrically conductive paths or traces (not shown). The metallized pattern on the upper and lower surfaces 120, 130 of the insulating base 110 may be formed by photolithography, electroplating, etching, screen printing, or other similar techniques. The optical devices and/or electrical components may be mounted to and electrically connected to the conductive metallized pattern on the upper surface 120 of the insulating base 110.

[0028] At least one electrical lead 170 is attached, e.g., by brazing, to the lower metallized surface 130 of the insulating base 110, and is connected to the upper metallized surface 120 of the insulating base 110 via the first plurality of filled holes 117. The electrical leads 170 are adapted to communicate signals from the optoelectronic and/or electrical components housed inside the low-profile package 100 to components located external to the package 100 on, for example, a printed circuit board. The leads 170 may be circular or rectangular in cross-section. Preferably, the electrical leads 170 are arranged as an array of leads 170, and may be located at any location on the lower surface 130 of the insulating base 110. The insulating base 110 may be operatively coupled to sockets in the printed circuit board (not shown) via the electrical leads 170. Alternatively, the insulating base 110 may be operatively coupled to the printed circuit board using solder connections such as, for example, ball grid array connections and/or a flex circuit.

[0029] The metal sealing member 140 may be sealably attached to the upper metallized surface 120 of the insulating base 110 using an adhesive layer 149 disposed between the metal sealing member 140 and the upper surface 120 of the insulating base 110. The metal layer on the upper surface 120 of the insulating base 110 may be etched, grinded, and/or polished to provide a substantially flat contact surface for attachment of the metal sealing member 140. The metal sealing member 140, which may be formed of Kovar™ or any other similar metallic material, includes a top wall 141, a bottom wall 142, an outer wall 143, and an inner wall 144.

[0030] Preferably, the metal sealing member 140 is a sealing ring having a generally circular cross-sectional shape between the outer wall 143 and inner wall 144. However, the metal sealing member 140 may have other shapes as well. For example, the metal sealing member 140 may have a generally oval cross-sectional shape between the outer wall 143 and inner wall 144. Still further, the metal sealing member 140 may have a polygonal shape such as a rectangular cross-sectional shape or a square cross-sectional shape between the outer wall 143 and inner wall 144.

Lastly, the thickness of the metal sealing member 140 may range from approximately 0.5 mm to approximately 2 mm. In this manner, the relatively thick outer wall 143 of the metal sealing member 140 encircles and protects the optoelectronic and/or electrical components located within an inner region of the metal sealing member 140.

[0031] The adhesive layer 149, which is basically a wafer-sized prefabricated bond, is disposed on the upper surface 120 of the insulating base 110. The adhesive layer 149 may include a brazing paste of, e.g., copper and/or silver, or a solder preform layer 149 formed of metal (e.g., a gold or tin preform). The bottom wall 142 of the metal sealing member 140 is then positioned on the adhesive layer 149 on the upper surface 120 of the insulating base 110. Through appropriate use of a brazing heat operation, the metal sealing member 140 is bonded to the upper surface 120 of the insulating base 110.

[0032] Referring back to Fig. 1, the substantially flat cover 150, which is preferably formed of Kovar™ or other suitable metal, is then hermetically sealed to the top wall 141 of the metal sealing member 140 to contain and fully enclose the optoelectronic and electrical components mounted to the upper surface 120 of the insulating base 110, and to thereby seal off the module package 100. Use of such a hermetically sealed cover 150 acts to keep out moisture, corrosion, and ambient air to therefore protect the generally delicate optoelectronic and electrical components housed inside the low-profile package 100.

[0033] Typically, the metal cover 150 is circular or cylindrical in shape. However, the metal cover 150 may have a square or rectangular shape instead depending on the shape of the metal sealing member 140. In other words, the shape of the metal cover 150 is generally complementary to the shape of the metal sealing member 140 so that the metal cover 150 can be hermetically sealed to the top wall 141 of the metal sealing member 140. For example, the metal cover 150 may be generally circular when the metal sealing member 140 has a generally circular cross-sectional shape between the

outer wall 143 and inner wall 144. Likewise, the metal cover 150 may be generally rectangular when the metal sealing member 140 has a generally rectangular cross-sectional shape between the outer wall 143 and inner wall 144. By enclosing and hermetically sealing the metal cover 150 to the insulating base 110, the optoelectronic and electrical components housed within the package 100 are kept in a controlled gaseous, liquid, or vacuum environment that protects them and prevents degradation in their performance and/or lifetime. In addition, the metal cover 150 is substantially flat to minimize the height or profile of the package 100, and thereby provide a higher density.

[0034] As shown in Fig. 1, the substantially flat metal cover 150 may be set back from the outer wall 143 of the metal sealing member 140. Alternatively, the substantially flat metal cover s may be substantially flush with the outer wall 143 of the metal sealing member 140. A hermetically sealed attachment of the substantially flat metal cover 150 to the metal sealing member 140 on the insulating base 110 may be established by, for example, seam welding, laser welding, resistance welding, soldering, glazing, etc.

[0035] Referring to Fig. 4, the substantially flat metal cover 150 includes a transparent portion 160 such as, for example, a flat glass window, ball lens, aspherical lens, or GRIN lens. The optoelectronic components are mounted to the insulating base 110 within the low-profile package 100 in a manner such that light is able to pass to or from them through the transparent portion 160. Typically, the transparent portion 160 is formed of glass, ceramic, or plastic. To avoid effects on the optoelectronic and/or electrical components housed within the low-profile package 100, the transparent portion 160 of the substantially flat cover 150 may be provided with an antireflection coating to reduce optical loss and back-reflection. The transparent portion 160 of the substantially flat metal cover 150 is aligned with the beam emergence side of the optoelectronic device 200, so that the optoelectronic device 200 can be optically coupled to external components such as, for example, an

optical fiber or any element that requires optical alignment with other optical devices, through the transparent portion 160.

[0036] The insulating base 110 may form the bottom of the low-profile package 100, thus making a completely self-contained package 100. Alternatively, the insulating base 110 may include one or more submounts that carry the optoelectronic and/or electrical components. In other words, the optoelectronic and/or electrical components may be mounted directly to the upper surface 120 of the insulating base 110, or may be mounted to submounts that are attached to the insulating base 110.

[0037] As illustrated in Fig. 4, an active optical device 200 and its associated integrated circuit chip 220, a passive optical device 300, and various other electrical components 310, 320 are located within an inner region of the metal sealing member 140. As is well known, these optical and/or electrical components may be mounted to the upper surface 120 of the insulating base 110 by pick-and-place techniques commonly used in the electronics industry, and attached to the insulating base 110 by adhesive bonding, soldering, welding, gluing, or other similar method. Because the insulating base 110 is substantially planar, the pick-and-place automation may use relatively simple machine vision for accurate placement and alignment of the various components.

[0038] In the embodiment illustrated in Fig. 4, the insulating base 110 serves as both a mounting surface for the various optical and/or electrical components as well as the bottom or header of the low-profile package 100 itself. As a result, a smaller, higher-performance, and cost-effective enclosure may be realized. In particular, the low-profile package 100 may be assembled in a relatively uncomplicated manner by simply attaching the substantially flat metal cover 150 to the base 110 upon which the optoelectronic components are mounted to thereby create a hermetic enclosure. In addition, due to the substantial flatness of the metal cover 150, standard tooling may be used to manufacture the substantially flat metal cover 150, thus resulting in a manufacturing process that is less complex and inexpensive.

[0039] To ensure low parasitic effects (e.g., capacitance, resistance, and/or inductance) and reduced interconnect lengths for enhanced electrical performance, it is advantageous to mount the active optical device 200 and the integrated circuit 220 close to each other inside the low-profile package 100. As a result, higher electrical performance may be achieved in smaller packages at low cost. This configuration is particularly advantageous for high-speed applications, e.g., 10 Gbps and greater, because extraneous wiring that may limit the high-speed operation of the optoelectronic package 100 is eliminated.

[0040] Optically active devices 200 include any well known or future devices that generate light when stimulated, that sense light, convert light to electrical signals, or that condition light. For example, active optical devices 200 may include light emitters (e.g., vertical cavity surface-emitting lasers (VCSEL), Fabry-Perot (F-P) lasers, distributed-feedback (DFB) lasers, light emitting or sensing diodes, and the like), light sensors (e.g., photodetectors), and optical modulators. The integrated circuit 220 is any chip suitable for applying an electrical signal to the active optical device 200 to activate and control the device 200 such as, for example, a microprocessor, a driver chip for a transmitter device, or a transimpedance amplifier chip for a receiver device. Implementation of the microprocessor, driver, or transimpedance amplifier integrated circuit 220 is well known, and thus will not be further described.

[0041] In addition to the active optical device 200 and its associated integrated circuit 220, other optical and/or electrical components such as a mirror 300, thermistor 310, capacitor 320, etc. may be mounted to the insulating base 110 and housed inside the low-profile package 100. It is to be understood, however, that other optical and/or electrical devices besides those mentioned above may be mounted to the insulating base 110 as well.

[0042] In sum, the low-profile optoelectronic package 100 of the present disclosure may be produced in an automated batch process that is similar to the batch processes

used in manufacturing integrated circuits. In addition, the low-profile package 100 may be manufactured cost-effectively because expensive tooling is eliminated. Lastly, the low-profile optoelectronic package 100 offers the simultaneous advantages of high-speed electrical operation, hermeticity, effective heat sinking, and high mechanical stability.

[0043] In the foregoing description, the disclosed structures and manufacturing methods have been described with reference to exemplary embodiments. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of this disclosure. The above specification and figures accordingly are to be regarded as illustrative rather than restrictive. It is therefore intended that the present disclosure be unrestricted by the foregoing description and drawings, except as may appear in the following appended claims.